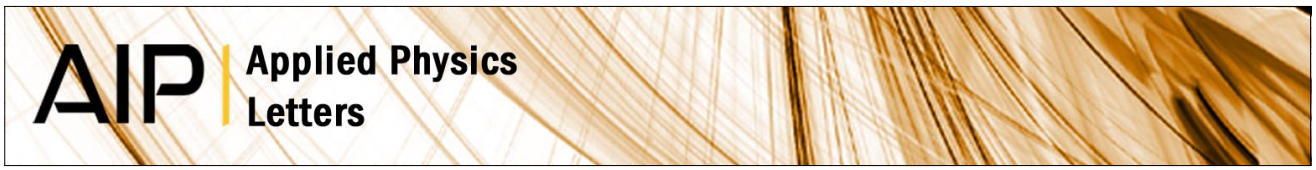

High program efficiency of p-type floating gate in n-channel split-gate embedded flash memory

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High program efficiency of *p*-type floating gate in *n*-channel split-gate embedded flash memory

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This work proposes a novel *p*-type boron-doped floating gate for *n*-channel split-gate flash memory. A lower program voltage, with a programming time of 7 μs, results in five times of the conventional source-side injection programming efficiency, a 5% wider program/erase window, and more reliable endurance characteristics. Additionally, a 2 Mbit embedded flash Intellectual Property (IP) has been successfully implemented and statistically compared. The lower program voltage reduces concerns around the high-voltage decoder, the charge pump efficiency, and the array efficiency beyond 90 nm nodes. The new *p*-doped split-gate structure provides a very promising solution for advanced embedded split-gate flash memory beyond the 90 nm node. © *2008 American Institute of Physics*. [DOI: 10.1063/1.3023057]

Unlike the stack-gate flash memory cell, split-gate flash cell usually utilizes source-side injection (SSI)[1–4] in the program operation and poly-to-poly field tunneling in the erase operation.[1–5] The advantages of SSI are higher programming efficiency, lower program current, and better array efficiency for logic-based embedded flash applications. Moreover, not only is the source coupling ratio limited by the continuous scaling down of the cell channel length, but also the reduction in the SSI program voltage is constrained by the need for maximum electrical field in channel hot electron generation.

A few stack-gate flash memories using *p*-type floating gates (FGs) have been reported and characterized by Chung *et al.*[6] and Wu *et al.*[7] Earlier studies showed that the *p*-FG cell has a higher programming speed and retention by the drain-side program of channel hot electron injection. This study proposes a proper boron-doped FG in place of the common *n*-doped FG in split-gate flash cells. The change in work function of the floating poly-Si causes the *p*-type FG split-gate cell to have a higher program efficiency in the SSI mechanism.[8,9] The cell also has a tighter program distribution than the *n*-type FG split-gate cell and better endurance characteristics in 2 Mbit flash memory. These advantages result in lower program operation voltages[10,11] and better flash reliability, making the split-gate flash more scalable and effective in 90 nm embedded flash memory and beyond.

The experimental split-gate cells use the double polysilicon 0.15 μm complementary metal-oxide semiconductor embedded flash process, and the *n*-type and *p*-type FG cells were fabricated for characterization and comparison. Additionally, the experimental cells have a bowl-shaped FG for field-enhanced tunneling in erase operation, as displayed in Fig. 1(a).[12] The main cell process steps are the following. First, the thin coupling oxide (~85 A) was then thermally grown; then, the intrinsic polysilicon was deposited on top of it as the FG. A disposable nitride layer was deposited immediately and photo and nitride etch processes were performed to separate the FG regions. Subsequently, different dopant species were implanted for the forming of *n*-doped or *p*-doped FG in different experimental samples. The next step was thermal polysilicon oxidation and a bowl-shaped FG was produced. Interpolyoxide (150 A) was deposited to isolate the FG and as the tunneling oxide used in erase operation. The second polysilicon was finally deposited and patterned to form the control gate (CG) of the split-gate cell. In a chip level study, 2 Mbit chips were fabricated using the same 0.15 μm cell process sequence and split conditions. The memory array contains 512 word lines and 64 bit lines with a total of 16 Input/Output (I/O)s and four banks of subarrays.

The three experimental samples include one *n*-doped FG condition and two *p*-doped FG conditions. The *n*-doped sample underwent FG implantation of 2×10^{14} cm^{-2} phosphorus and the *p*-doped samples underwent implantation of 2×10^{14} and 4×10^{14} cm^{-2} in boron, respectively. The split-gate memory cells are all performed with the same erase operation of poly-to-poly field enhanced tunneling, and the erase conditions are all maintained as V_{CG}=13.3 V, V_S

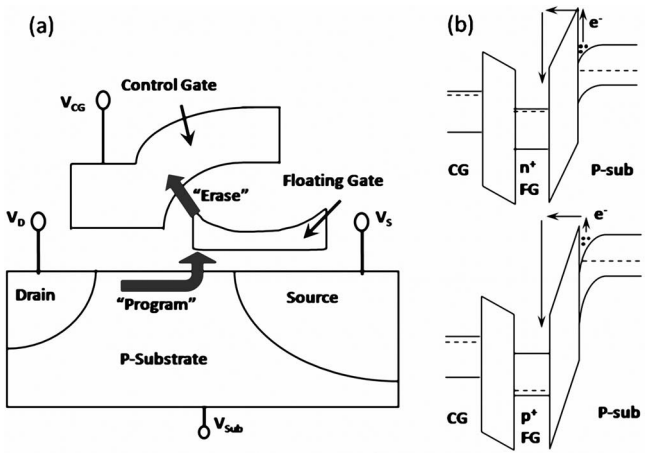

FIG. 1. (a) The cross-sectional view of split-gate memory. (b) The band diagram under the same program condition of the *n*-doped and *p*-doped FG split-gate cells.

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TABLE I. Program conditions of split-gate memory cells. The current criterion for successful program is around 3 μA.

FG doping type	FG doping concentration	Program condition	
		V_S (V)	V_{CG}/V_D /time
n	2×10^{14} cm^{-2} phosphorus	11.2	1.8 V/0.7 V/100 μs
n	2×10^{14} cm^{-2} boron	9.1	1.8 V/0.7 V/100 μs
p	4×10^{14} cm^{-2} boron	8.6	1.8 V/0.7 V/100 μs

$=V_D=0$ V, and $t=1$ ms. The read operation is biased at $V_{CG}=3$ V, $V_S=0$ V, and $V_D=0.8$ V. Both *n*-doped and *p*-doped FG split-gate cells are programmed by SSI but use different programming operation conditions, which are summarized in Table I. The difference between the work function of the *p*-doped FG and the conventional *n*-doped FG is such that the *p*-doped FG split-gate cell has a larger vertical electric field than the *n*-doped FG during the SSI program operation [Fig. 1(b)]. The change in the field causes the hot electrons in the channel to have a higher probability of injection in the *p*-doped FG. Figure 2 shows the program characteristics of the three FG samples. It clearly indicates that the *p*-doped FG cells have a higher program speed than the *n*-doped FG cell. Moreover, further comparing the two doping concentrations of the *p*-doped FG cells reads that the more heavily *p*-doped FG also has 2.5 times higher programming speed than the more lightly *p*-doped FG because the coupling ratio is higher. In summary, *p*-doped FG split-gate cells with a proper concentration can support more efficient SSI program operation than the *n*-doped FG split-gate cell, reducing the high voltage required in the program operation. To evaluate statistically the operation window, Fig. 3 plots the 2 Mbit cumulative distributions of programmed bit cell currents for different FGs. As a result, the *p*-doped FG split-gate cells have a much tighter programmed cell current distribution for the same program condition. In addition, the programming/erasing window is wider for a given same initial erase current. While the same program voltages were applied on the 2 Mbit cells, because of the *p*-doped FG cell has better program efficiency than the *n*-doped FG cell, the tailing bits will be converged quickly within a limited program time, such as 100 μs. Consequently, the program voltage and high voltage requirement in chip design can be reduced or the program time can be shorter. In terms of the endurance characteristics, after over 600 K cycles, the *p*-doped FG split-gate cells degrade much less than the *n*-doped FG cell, as shown in Fig. 4. In this cycling characterization, the degradation of the *p*-doped FG cells drops by 20% of the cell current but the *n*-doped FG cell exhibits a cell current degradation of over 25%; this difference is caused by severe oxide damage associated with the 2 V higher program operation in the *n*-doped FG cells. In conclusion, the new *p*-type FG exhibits better program performance and more reliable endurance characteristics; these advantages enable the split-gate flash cells to be operated at a lower program voltage, with lower power consumption, and longer cycling stresses.

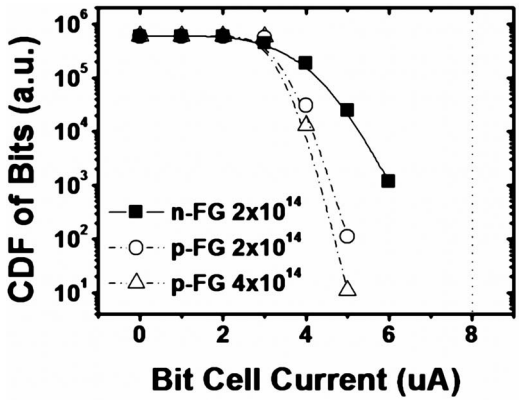

FIG. 3. The cumulative distribution of 2 Mbit cells at programmed state. The programming conditions are $V_S/V_{CG}/V_D$/time =8 V/1.8 V/0.7 V/100 μs for *p*-type and *n*-type cells.

A *p*-doped FG split-gate memory cell has been successfully demonstrated. The new cell shows high program efficiency, good endurance characteristics, and superior bit cell current distribution in 2 Mbit memory array. The *p*-doped FG cell supports >2 V lower SSI program operating voltage. The *p*-type boron-doped FG cell exhibits efficient program performance with a wider erase operation window and better endurance than the conventional *n*-type FG cell. Based on these advantages, the new structure makes the split-gate cell more scalable and effective in 90 nm embedded flash memory and beyond.

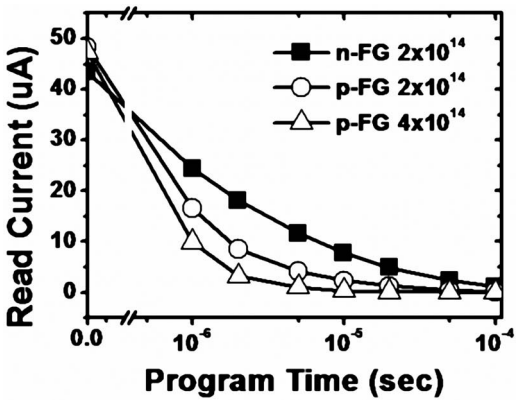

FIG. 2. Comparison of the programming characteristics for split-gate cells with FG at different types of doping and concentrations. The read condition is $V_{CG}/V_S/V_D=3$ V/0 V/0.8 V.

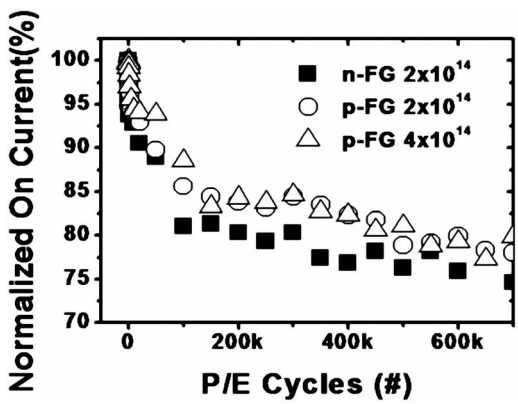

FIG. 4. The normalized on-current for endurance characteristics of the split-gate cells with *n*-type and *p*-type FG dopings.

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